Fan-Out Wafer and Panel Level Packaging Trends

4th Panel Level Consortium Symposium

8th September 2022

Gabriela Pereira
Fan-Out Wafer and Panel Level Packaging Trends – 4th Panel Level Consortium Symposium

- Author & Yole Group Presentation
- Fan-out Packaging Market & Technology
- Fan-out Panel Level Packaging adoption
- Conclusions
- Q&A

Market forecasts extracted from Yole’s Advanced Packaging Market Monitor Q2 2022
AUTHOR & YOLE GROUP PRESENTATION
Gabriela PEREIRA, Technology and Market Analyst

Gabriela Pereira is in the packaging team within the Semiconductor, Memory and Computing Division at Yole Intelligence (Yole). Gabriela focuses on Advanced Packaging platforms, develops technology & market reports, and is engaged in dedicated custom projects. Gabriela’s experience in the semiconductor field includes working at Amkor Technology, first for her master's thesis and then as an R&D Engineer.

Gabriela holds a master’s degree in Metallurgical and Materials Engineering from the University of Porto, Portugal.

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Yole's market forecast model is based on the matching of several sources:

Comparison with existing data
- Monitoring of corporate communication
- Using other market research data
- Yole's analysis (consensus or not)

Comparison with prior Yole reports
- Recursive improvement of dataset
- Customer feedback

Preexisting information

Top-down approach
- Aggregate of market forecasts
  @ System level

Top-down approach
- Aggregate of market forecasts
  @ Semiconductor device level

Bottom-up approach
- Ecosystem analysis
- Aggregate of all players’ revenues
  @ System level

Bottom-up approach
- Ecosystem analysis
- Aggregate of key players’ revenues
  @ Semiconductor device level

Primary data
- Reverse costing
- Patent analysis
- Annual reports
- Direct interviews

Secondary data
- Press releases
- Industry organization reports
- Conferences

Information Aggregation
Fan-Out Packaging Technology
YOLE’S DEFINITION OF FAN-OUT PACKAGE

Different ways of classification

Fan-out Package

A mold compound is used to embed the chip.
Connections are fanned out of the chip scale area
No IC substrate (PCB type) used for fanning out from the chip area

Classification by process flow
- Chip-First
- Face-up
- Face-down
- Chip-Last

Classification by I/O density & L/S
- Core FO
- HD FO
- UHD FO

Classification by carrier type
- Wafer
- Panel

TOP THREE MARKET DRIVERS
- High-performance computing
- High-end mobile & consumer APE packaging
- Radar/5G devices (Potentially) RF/AiP packaging
FAN-OUT PACKAGING SEGMENTATION: APPLICATIONS
Core FO, HD FO & UHD FO

- **Core FO**: Core fan-out
- **HD FO**: High-Density fan-out
- **UHD FO**: Ultra-High-Density fan-out

<table>
<thead>
<tr>
<th>RDL L/S Scaling (µm/µm)</th>
<th>I/O per package area (I/O per mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>≥20/20</td>
<td>∼1</td>
</tr>
<tr>
<td>15/15</td>
<td>≤1</td>
</tr>
<tr>
<td>10/10</td>
<td>≤2/2</td>
</tr>
<tr>
<td>5/5</td>
<td>≤2/2</td>
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<tr>
<td>1/2</td>
<td>≥10</td>
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</table>

- **IC Substrate**
  - IC Substrate
  - Application Processors (APE) + BB APE+DRAM
  - Fan-out on Substrate

- **Core FO**
  - BB, PMU/PMIC, RF
  - Codec, DC-DC, Wi-Fi

- **HD FO**
  - MEMS, CMOS Image Sensors, Fingerprint Sensors, Display Drivers
  - 15µm/15µm > RDL L/S > 5µm/5µm
  - 2-4 RDLs

- **UHD FO**
  - 15µm/15µm > RDL L/S > 5µm/5µm
  - 2-4 RDLs

- **Application Processors (APE) + BB APE+DRAM**
- **Fan-out on Substrate**

- **GPU, CPU, Memory (Wide IO, etc...)**
- **High Bandwidth Memories**
- **FPGA Processors + Memories**

- **RDL L/S < 5µm/5µm**
  - 3-6 RDLs
FAN-OUT PACKAGING SEGMENTATION: PLAYERS
Core FO, HD FO & UHD FO

Core FO: Core fan-out
HD FO: High-Density fan-out
UHD FO: Ultra-High-Density fan-out

I/O per package area (I/O per mm²)

RDL L/S Scaling (μm/μm)

Fan-out on Substrate

New entrants and potential up-and-coming players
Fan-Out market will grow at a 11% CAGR 2021-2027

2021
- Core FO 20%
- HD FO 33%
- UHD FO 47%
- Total Revenue: $2.1B

2027
- Core FO 11%
- HD FO 37%
- UHD FO 52%
- Total Revenue: $4B

2021 Fan-Out Packaging Market Shares

- TSMC 69%
- Samsung Electronics 1%
- Amkor 3%
- ASE/w SPIL 20%
- Huatian $9 0.40%
- Nepes Laweh 2%
- PTI 1%
- JCET 4%
- Samsung 1%

Fan-Out Panel Level Packaging Adoption
WHAT IS THE MAIN MOTIVATION FOR FOPLP INSTEAD OF FOWLP?

Motivations

- Cost reduction by usage of larger carrier → main driver
- Advantageous for high volumes and large package sizes.
- Flexibility in the manufacturing flow.
- Capability for panel manufacturers (PCB/substrate suppliers) to use existent equipment and panel handling experience.
- Allows RDL layers to be easily built using polymeric films, which can provide flatness advantages and low package thicknesses.

Challenges

- Large investments are needed to develop panel lines, specially for wafer level manufacturers.
- Investment is only justified by high volume applications.
- Not an advantageous investment for small package size applications, once WLP can still take over.
- Resolution - manufacturers must define which type of panel to use i.e., PCB or glass.
- Qualification and reliability of new processes and materials.
- Not yet a mature technology.
FOGPLP BENEFITS: COST REDUCTION

- Price reduction is a key parameter for fan-out market growth. That price reduction can be achieved by reducing manufacturing cost, which is achieved by using larger carriers.

- Moving to panels could enable cost reduction up to 66% if the technology is ready and yields are higher than 90%.

*Cost estimations based on System Plus Consulting analysis and interviews with key players
 WHICH TYPE OF PANEL?
Size matters and so does type of the carrier

PCB and advanced substrate lines are quite diverse, but all are larger than 300mm wafers. Some OSATs already have experience with substrates and therefore naturally use these formats for FO panels.

Wafer-based FO can benefit from advanced mid-process equipment able to build small packages and features. Total area is limited though.

Glass panels – glass panels for LCD industry are now reaching gigantic sizes (Gen. 8 are 2200mm x 2500mm for instance) but many players have older-generation lines that could be large enough to address the packaging market.
**FAN-OUT PACKAGING ON PANELS - TECHNICAL CHALLENGES**

1. **Panel warpage**
   - Heterogenous materials
   - Bigger substrate size
   - Low shrinkage and modified CTE required

2. **Assembly of die/accuracy**
   - Die placement accuracy more challenging to control with bigger substrate size.
   - Impact of throughput to pick-and-place die on panel means an impact on yield and cost

3. **Impact of materials**
   - Dielectric materials: spin-on vs. dry
   - Photo-resist: how to apply it? Slit coating?
   - Molding compound

4. **Equipment manufacturability**
   - Dielectric materials: How to deposit?
     - Spin coating? Lamination tools?
     - Metal plating: How to sputter the seed layer?
     - Solder ball placement
     - What level of inspection is required to confirm accuracy, materials, and interconnect reliability?
MANUFACTURERS OF FAN-OUT PACKAGING

Key players running FOWLP & FOPLP production and new entrants

**Production**

- FOWLP ONLY
  - JCET
  - TSMC
  - Amkor Technology
  - SPIL
  - NXP
  - Infineon
  - HUA TIAN

- FOWLP + FOPLP
  - Samsung
  - ASE Group
  - Netez

- FOPLP ONLY
  - PowerTech Technology Inc.

**New Entrants***

- FOWLP ONLY
  - LB Semicon
  - Skywater

- FOWLP + FOPLP
  - ESWIN
  - InnoLux
  - Unimicron

- FOPLP ONLY
  - RTI Technology Inc.

*Non-exhaustive list of players

*Potential only
## MANUFACTURERS OF FOPLP

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<tr>
<th>Panel Size</th>
<th>≤ 2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
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<td>&gt; 2/2 µm</td>
<td>&gt; 2/2 µm</td>
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<tr>
<td></td>
<td>PMIC, Codec, SiP</td>
<td>APU</td>
<td>CPU, GPU, ASIC*</td>
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<td>line from SEMCO</td>
<td>APU</td>
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<td>CPU, GPU, ASIC*</td>
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<td>PMIC, RF, FEM</td>
<td>APU, SiP</td>
<td>CPU, GPU, ASIC*</td>
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- **M-Series, nPLP, nPoP, nSiP**
- **CHIEFS, CLIP, PiFO (PoP), BF²O**
- **SAMSUNG FOPLP**
- **M-Series Future: FOSiP, FOPoP, FoCoS**

*Potential

Min. L/S  New applications

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FOPLP production will keep growing as more players adopt the technology for cost reasons. However, FOWLP will continue to dominate the fan-out industry as it is a mature technology.
FOPLP revenues are set to grow at a 23.8% CAGR but FOWLP will continue to be the main platform with 10.5% CAGR 2021-2027
Currently, the biggest market portion of FOPLP is correspondent to Core FO as the main application driver is PMIC.

HD FO will gain traction as FOPLP will be increasingly adopted in application processors. FOPLP adoption in UHD FO applications will not start before 2023. Its adoption is driven mainly by the large package trend and the cost benefit, but it will depend on the technology maturity, yield and reliability.
Fan-out market share is experiencing a high expansion, driven by HD FO and UHD FO platforms.

FOPLP can provide cost advantages compared to FOWLP, especially in large-die chip manufacturing. Though, the technical, financial and supply chain hurdles are still around.

FOPLP production will keep growing as more players adopt the technology for cost reasons. However, FOWLP will continue to dominate the fan-out industry as it is a mature technology.

Analyst point of view...

FOPLP is still on hold until volumes are big enough to address the need for the huge conversion from wafer to panel carriers.

Adoption of FOPLP is driven mainly the cost benefit, but it will depend on the technology maturity, yield and reliability...
CONCLUSIONS

Thank you for your attention!

Any questions? gabriela.pereira@yolegroup.com

Q & A